IN THE CLAIMS:

Please amend claims 1-14 as follows:

1. (Currently Amended) A data processing device comprising:

a cache memory comprising a plurality of cache lines;

a cache control part for controlling the cache memory; and

a memory control part accessible to [[a]] an external memory in response to a cache mishit of the cache memory,

wherein in ~~having~~ access to [[a]] the external memory burstable in response to a cache mishit, the memory control part forms first information [[for]] indicating a burst length of the external memory and a starting address of at least one burst operation of the burst length and ~~it can~~ controls ~~a single or plurality of~~ said burst operation[[s]] necessary to join ~~obtain a~~ data retrieved from the starting address into a data entity with a length meeting ~~a~~ with one cache line length of one of the cache lines ~~according to the first information~~, and

the cache control part ~~can~~ controls a cache fill operation of filling data ~~acquired~~ joined in ~~the single or plurality of~~ said burst operation[[s]] into the cache memory ~~so as to locate~~ by arranging the data in order of addresses according to the first information to corresponding locations in said one of the cache lines independently whether the starting address is a top address of said one of the cache lines or not.

2. (Currently Amended) The data processing device according to claim 1, wherein in the cache fill operation, the cache control part receives inputs of address information in a cache mishit, the first information, and a synchronization signal synchronous with a delimiter of the data ~~acquired~~ joined in said burst operation[[s]] by the memory control part, and the cache control part generates a cache fill address for determining a data order of cache fill in synchronism with the synchronization signal in order to ~~perform~~ write ~~control for~~ into the cache memory starting from the address information in a range ~~of a~~ as the burst length ~~meant by~~ indicated in the first information.

3. (Currently Amended) The data processing device according to claim 1, wherein in ~~having~~ access to [[a]] the external memory in a plurality of burst operations in response to a cache mishit, the memory control part controls a first burst operation starting from a data

location at an address in the cache mishit therein ~~a first burst operation,~~ and ~~the memory control part controls~~ a subsequent burst operation starting from a top of a boundary of a data block defined by ~~the~~ a burst length thereof ~~in subsequent burst operations~~.

4. (Currently Amended) A data processing system comprising:

a data processing device having a CPU and a cache memory; and

a memory connected to the data processing device, the memory being burstable and configuring a main memory for the cache memory,

wherein the cache memory has a plurality of cache lines each of which has length of L bytes,

the memory is burstable in a range of a burst length in bytes, where the range is defined as L times one over two to the n-th power (n is ~~a natural~~ a positive integral number), and

the data processing device forms first information [[for]] indicating a burst length of the memory equal to a cache line length of the cache memory ~~in response to a cache mishit of the cache memory~~ and a starting address of at least one burst operation of the burst length, the data processing device ~~allows the memory into~~ controls said burst operation[[s]] ~~for a single or plurality of times~~ necessary to join ~~obtain a~~ data retrieved from the starting address into a data block with a length meeting ~~a~~ with said cache line length of one cache line of the cache memory ~~according to the first information~~, and

the data processing device ~~performs~~ controls ~~of~~ returning of data of L bytes ~~thereby obtained~~ to the cache memory so as to arrange the data in order of addresses according to the first information to corresponding locations in said one of the cache lines independently whether the starting address is a top address of said one cache line or not.

5. (Currently Amended) A data processing system comprising:

a data processing device having a CPU and a cache memory; and

a plurality of memories connected to the data processing device, the plurality of memories being burstable and configuring a main memory for the cache memory,

wherein the cache memory has a plurality of cache lines each of which has length of L bytes,

each of the plurality of memories is burstable in a range of a burst length in bytes,

where the range is defined as L times one over two to the n-th power (n is ~~a natural~~ a positive integral number), and the burst length is ~~allowed to be~~ individually set in each of the plurality of memories by the data processing device, and

the data processing device establishes ~~a memory~~ two or more of the plurality of memories with data ~~in a cache mishit as an object~~ to be accessed in response to a cache mishit of the cache memory, and for each of said two or more of the plurality of memories, the data processing device ~~performs controls in which the data processing device~~ forms first information [[for]] indicating a burst length of the memory equal to ~~be accessed to~~ a cache line length of the cache memory and a starting address of at least one burst operation of the burst length, the data processing device ~~allows the memory into~~ controls said burst operation[[s]] ~~for a single or plurality of times~~ necessary to join ~~obtain~~ a data retrieved from the starting address into a data block with a length meeting ~~a~~ with said cache line length of one cache line of the cache memory ~~according to the first information~~, and

the data processing device returns data of L bytes ~~thereby obtained so as~~ to ~~locate~~ arrange the data in order of addresses according to the first information to corresponding locations in said one of the cache lines independently whether the starting address is a top address of said one cache line or not.

6. (Currently Amended) The data processing system according to claim 4, wherein the data processing device ~~performs~~ controls ~~in which~~ data joined ~~acquired~~ in the burst operation[[s]] ~~for the single or plurality of times is~~ to be filled in the cache memory according to the first information.

7. (Currently Amended) The data processing system according to claim 4, wherein in cache fill operations, the data processing device generates a synchronization signal synchronous with a delimiter of the data ~~axquired~~ joined from the memory in said [[the]] burst operation[[s]], and the data processing device generates a cache fill address for determining a data order of cache fill in synchronism with the synchronization signal in order to ~~perform~~ write ~~control for~~ into the cache memory starting from the address information in a range ~~of a~~ as the burst length ~~meant by~~ indicated in the first information.

8. (Currently Amended) The data processing system according to claim 4, wherein in ~~having~~ access to [[a]] the memory in a plurality of burst operations in response to a cache mishit, the data processing device controls a first burst operation starting from a data location at an address in the cache mishit therein ~~a first burst operation,~~ and ~~the data processing device controls~~ a subsequent burst operation starting from a top boundary of a data block defined by ~~the~~ a burst length thereof ~~in subsequent burst operations~~.

9. (Currently Amended) A data processing system comprising:

a CPU;

a cache memory having a plurality of cache lines and accessible by the CPU;

a cache control part for controlling the cache memory;

a memory control part accessible to a memory in response to a cache mishit of the cache memory; and

a memory connected to the memory control part~~, the memory~~ and being burstable,

wherein ~~having~~ in access to the memory in response to a cache mishit, the memory control part generates first information [[for]] indicating a burst length of the memory and a starting address of at least one burst operation of the burst length~~,~~ and ~~the memory control part can~~ controls ~~a single or plurality of~~ said burst operation[[s]] necessary to join ~~obtain a~~ data wraparounded from the starting address into a data entity with a length meeting ~~a~~ with one cache line length of one of the cache lines ~~according to the first information~~, and

the cache control part ~~can~~ controls a cache fill operation of filling data ~~acquired~~ joined in ~~the single or plurality of~~ said burst operation[[s]] into the cache memory ~~so as to locate~~ by arranging the data in order of addresses ~~by wraparound~~ according to the first information to corresponding locations in said one of the cache lines independently whether the starting address is a top address of said one of the cache lines or not.

10. (Currently Amended) The data processing system according to claim 9, wherein in the cache fill operation the cache control part receives inputs of address information in a cache mishit, the first information, and a synchronization signal synchronous with a delimiter the data ~~acquired~~ joined in said burst operation[[s]] by the memory control part, the cache control part ~~controls~~ wraparounds data blocks starting from the address

information in a range ~~of a~~ as the burst length ~~meant by~~ indicated in the first information, and the cache control part generates a cache fill address for determining a data order of cache fill in synchronism with the synchronization signal.

11. (Currently Amended) The data processing system according to claim 10, wherein in ~~having~~ access to [[a]] the memory in a plurality of burst operations in response to a cache mishit, the memory control part controls a first burst operation by wraparounding data blocks starting from a data location at an address in the cache mishit therein ~~a first burst operation,~~ and ~~the memory control part controls~~ a subsequent burst operation starting from a top boundary of a data block defined by ~~the~~ a burst length thereof ~~in subsequent burst operations~~.

12. (Currently Amended) The data processing system according to claim 5, wherein the data processing device ~~performs~~ controls ~~in which~~ data joined ~~acquired~~ in the burst operation[[s]] ~~for the single or plurality of times is~~ to be filled in the cache memory according to the first information.

13. (Currently Amended) The data processing system according to claim 5, wherein in cache fill operations, the data processing device generates a synchronization signal synchronous with a delimiter of the data ~~axquired~~ joined from the memory in said [[the]] burst operation[[s]], and the data processing device generates a cache fill address for determining a data order of cache fill in synchronism with the synchronization signal in order to ~~perform~~ write ~~control for~~ into the cache memory starting from the address information in a range ~~of a~~ as the burst length ~~meant by~~ indicated in the first information.

14. (Currently Amended) The data processing system according to claim5, wherein in ~~having~~ access to [[a]] the memory in a plurality of burst operations in response to a cache mishit, the data processing device controls a first burst operation starting from a data location at an address in the cache mishit therein ~~a first burst operation,~~ and ~~the data processing device controls~~ a subsequent burst operation starting from a top boundary of a data block defined by ~~the~~ a burst length thereof ~~in subsequent burst operations~~.